AMENDMENTS TO THE CLAIMS

Please amend the claims as shown below. A complete listing of all pending claims is presented.

1. (Original) A phase-locked loop circuit comprising:

a phase comparison means for detecting a size of a leading phase or a delayed phase of a feedback signal with respect to a reference signal and outputting a leading phase signal having a pulse width corresponding to the size of the leading phase or a delayed phase signal having a pulse width corresponding to the size of the delayed phase;

a smoothing means for smoothing the leading phase signal or the delayed phase signal output from the phase comparison means and outputting the result as a control signal;

a superposing means for superposing the leading phase signal or the delayed phase signal output from the phase comparison means on the control signal; and

an oscillation circuit for receiving the control signal superposed with other signals by the superposing means and outputting the feedback signal of a frequency corresponding to the control signal to the phase comparison means.

2. (Original) A phase-locked loop circuit as set forth in claim 1, wherein the superposing means includes a capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the control signal of the smoothing means at another terminal.

3. (Original) A phase-locked loop circuit as set forth in claim 2, wherein

the smoothing means includes

a current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal and

a filter for outputting said control signal obtained by smoothing the output current from the current outputting means.

4. (Original) A phase-locked loop circuit as set forth in claim 2, wherein

the smoothing means includes

a current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal,

a series circuit having a resistor and a capacitor receiving the output current from the current outputting means, and

a noise filter for receiving the voltage of the series circuit and outputting said control signal after removing noise components included in the voltage.

5. (Original) A phase-locked loop circuit as set forth in claim 4, wherein

the current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

6. (Original) A phase-locked loop circuit as set forth in claim 2, wherein

the smoothing means includes

a first current outputting means and a second current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal,

a series circuit having a resistor receiving the output current from the first current outputting means and a capacitor receiving a current of the resistor and the output current from the second current outputting means, and

a noise filter for receiving the voltage of the series circuit and outputting said control signal after removing noise components included in the voltage.

7. (Original) A phase-locked loop circuit as set forth in claim 6, wherein

the first current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

8. (Original) A phase-locked loop circuit as set forth in claim 6, wherein

the second current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

9. (Original) A phase-locked loop circuit as set forth in claim 1, wherein

the phase comparison means activates or deactivates outputs of the leading phase signal and the delayed phase signal to the superposing means according to a mode selecting signal.

10. (Original) A phase-locked loop circuit as set forth in claim 1, wherein

the phase comparison means adjusts pulse amplitudes of the leading phase signal and the delayed phase signal according to a pulse amplitude adjusting signal.

11. (Original) A phase-locked loop circuit as set forth in claim 1, wherein

the phase comparison means selects at least one leading phase signal or delayed phase signal from a plurality of the leading phase signals or the delayed phase signals according to a pulse amplitude adjusting signal and outputs it to the superposing means, and

the superposing means includes at least one capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an the current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

12. (Original) A phase-locked loop circuit as set forth in claim 1, wherein

the phase comparison means adjusts pulse widths of the leading phase signal and the delayed phase signal according to a pulse width adjusting signal.

13. (Currently amended) A phase-locked loop circuit comprising of a leading phase or a delayed phase of a feedback signal with respect to a reference signal and outputting a leading phase signal having a pulse width corresponding to the size of the leading phase or a delayed phase signal having a pulse width corresponding to the size of the delayed phase,

a smoothing means for smoothing the leading phase signal or the delayed phase signal output from the phase comparison means and outputting the result as a control signal,

a bias signal generating means for outputting a first bias signal and a second bias signal corresponding to the control signal,

a noise filter for removing noise components included in the first bias signal and the second signal,

a first superposing means for superposing the leading phase signal or the delayed phase signal output from the phase comparison means on the first bias signal,

a second superposing means for superposing the leading phase signal or the delayed phase signal output from the phase comparison means on the second bias signal, and

an oscillation circuit which includes a plurality of delay stages for exchanging and outputting a first current variable according to the first bias signal superposed with other signals by the first superposing means and a second current variable according to the second bias signal superposed with other signals by the second superposing means according to levels of input signals, feeds back an output signal of a last delay stage to an input of a first delay stage, and outputs an output signal of one of the delay stages as the feedback signal to the phase comparison means.

14. (Original) A phase-locked loop circuit as set forth in claim 13, wherein

the first superposing means includes a capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the first bias signal of the bias signal generating means at another terminal, and

the second superposing means includes a capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the second bias signal of the bias signal generating means at another terminal.

15. (Original)A phase-locked loop circuit as set forth in claim 13, wherein

the smoothing means includes

a current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal and

a series circuit having a resistor and a capacitor receiving the output current from the current outputting means, and

the bias signal generating means generates the first bias signal and the second bias signal according to a voltage of the series circuit.

16. (Original) A phase-locked loop circuit as set forth in claim 15, wherein

the current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

17. (Original) A phase-locked loop circuit as set forth in claim 13, wherein

the smoothing means includes

a first current outputting means and a second current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal and

a series circuit having a resistor receiving the output current from the first current outputting means and a capacitor receiving a current of the resistor and the output current from the second current outputting means, and

the bias signal generating means generates the first bias signal and the second bias signal according to a voltage of the series circuit.

18. (Original) A phase-locked loop circuit as set forth in claim 17, wherein the first current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

19. (Original) A phase-locked loop circuit as set forth in claim 17, wherein the second current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

20. (Original) A phase-locked loop circuit as set forth in claim 13, wherein the phase comparison means activates or deactivates outputs of the leading phase signal and the delayed phase signal to the superposing means according to a mode selection signal.

21. (Original) A phase-locked loop circuit as set forth in claim 13, wherein the phase comparison means adjusts amplitudes of the leading phase signal and the delayed phase signal according to a pulse amplitude adjusting signal.

22. (Original) A phase-locked loop circuit as set forth in claim 13, wherein

the phase comparison means selects at least one leading phase signal or delayed phase signal from a plurality of the leading phase signals or the delayed phase signals according to a pulse amplitude adjusting signal and outputs it to the first superposing means and the second superposing means,

the first superposing means includes at least one capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the first bias signal of the bias signal generating means at another terminal, and

the second superposing means includes at least one capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the second bias signal of the bias signal generating means at another terminal.

23. (Original) A phase-locked loop circuit as set forth in claim 13, wherein the phase comparison means adjusts pulse widths of the leading phase signal and the delayed phase signal according to a pulse width adjusting signal.

24. (Original) A delay-locked loop circuit comprising

a phase comparison means for detecting a size of a leading phase or a delayed phase of a feedback signal with respect to a reference signal and outputting a leading phase signal having a pulse width corresponding to the size of the leading phase or a delayed phase signal having a pulse width corresponding to the size of the delayed phase,

a smoothing means for smoothing the leading phase signal or the delayed phase signal output from the phase comparison means and outputting the result as a control signal,

a superposing means for superposing the leading phase signal or the delayed phase signal output from the phase comparison means on the control signal, and

a delay circuit for receiving the control signal superposed with other signals by the superposing means and the reference signal and outputting to the phase comparison means the feedback signal having a delay corresponding to the control signal relative to the reference signal.

25. (Original) A delay-locked loop circuit as set forth in claim 24, wherein

the superposing means includes a capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the control signal of the smoothing means at another terminal.

26. (Original) A delay-locked loop circuit as set forth in claim 25, wherein

the smoothing means includes

a current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal and

a filter for outputting a control signal obtained by smoothing the output current from the current outputting means.

27. (Original) A delay-locked loop circuit as set forth in claim 25, wherein

the smoothing means includes

a current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal,

a series circuit having a resistor and a capacitor receiving the output current from the current outputting means, and

a noise filter for receiving the voltage of the series circuit and outputting said control signal after removing noise components included in the voltage.

28. (Original) A delay-locked loop circuit as set forth in claim 27, wherein

the current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

29. (Original) A delay-locked loop circuit as set forth in claim 25, wherein

the smoothing means includes

a first current outputting means and a second current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal,

a series circuit having a resistor receiving the output current from the first current outputting means and a capacitor receiving a current of the resistor and the output current from the second current outputting means, and

a noise filter for receiving the voltage of the series circuit and outputting said control signal after removing noise components included in the voltage.

30. (Original) A delay-locked loop circuit as set forth in claim 29, wherein

the first current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

31. (Original)A delay-locked loop circuit as set forth in claim 29, wherein

the second current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

32. (Original) A delay-locked loop circuit as set forth in claim 24, wherein

the phase comparison means activates or deactivates outputs of the leading phase signal and the delayed phase signal to the superposing means according to a mode selection signal.

33. (Original) A delay-locked loop circuit as set forth in claim 24, wherein

the phase comparison means adjusts pulse amplitudes of the leading phase signal and the delayed phase signal according to a pulse amplitude adjusting signal.

34. (Original) A delay-locked loop circuit as set forth in claim 24, wherein

the phase comparison means selects at least one leading phase signal or delayed phase signal from a plurality of the leading phase signals or the delayed phase signals according to a pulse amplitude adjusting signal and outputs it to the superposing means, and

the superposing means includes at least one capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the control signal of the smoothing means at another terminal.

35. (Original) A delay-locked loop circuit as set forth in claim 24, wherein

the phase comparison means adjusts pulse widths of the leading phase signal and the delayed phase signal according to a pulse width adjusting signal.

36. (Original) A delay-locked loop circuit comprising

a phase comparison means for detecting a size of a leading phase or a delayed phase of a feedback signal with respect to a reference signal and outputting a leading phase signal having a pulse width corresponding to the size of the leading phase or a delayed phase signal having a pulse width corresponding to the size of the delayed phase,

a smoothing means for smoothing the leading phase signal or the delayed phase signal output from the phase comparison means and outputting the result as a control signal,

a bias signal generating means for outputting a first bias signal and a second bias signal corresponding to the control signal,

a noise filter for removing noise components included in the first bias signal and the second signal,

a first superposing means for superposing the leading phase signal or the delayed phase signal output from the phase comparison means on the first bias signal,

a second superposing means for superposing the leading phase signal or the delayed phase signal output from the phase comparison means on the second bias signal, and

a delay circuit which includes a plurality of delay stages for exchanging and outputting a first current variable according to the first bias signal superposed with other signals by the first superposing means and a second current variable according to the second bias signal superposed with other signals by the second superposing means according to

levels of input signals, inputs the reference signal to a first delay, and outputs an output signal of one of the delay stages as the feedback signal to the phase comparison means.

37. (Original) A delay-locked loop circuit as set forth in claim 36, wherein

the first superposing means includes a capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the first bias signal of the bias signal generating means at another terminal, and

the second superposing means includes a capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the second bias signal of the bias signal generating means at another terminal.

38. (Original) A delay-locked loop circuit as set forth in claim 36, wherein

the smoothing means includes

a current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal, and

a series circuit having a resistor and a capacitor receiving the output current from the current outputting means,

and the bias signal generating means generates the first bias signal and the second bias signal according to a voltage of the series circuit.

39. (Original) A delay-locked loop circuit as set forth in claim 38, wherein the current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

40. (Original) A delay-locked loop circuit as set forth in claim 36, wherein

the smoothing means includes

a first current outputting means and a second current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal and

a series circuit having a resistor receiving the output current from the first current outputting means and a capacitor receiving a current of the resistor and the output current from the second current outputting means, and

the bias signal generating means generates the first bias signal and the second bias signal according to a voltage of the series circuit.

41. (Original) A delay-locked loop circuit as set forth in claim 40, wherein the first current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

42. (Original) A delay-locked loop circuit as set forth in claim 40, wherein the second current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

43. (Original) A delay-locked loop circuit as set forth in claim 36, wherein the phase comparison means activates or deactivates outputs of the leading phase signal and the delayed phase signal to the superposing means according to a mode selection signal.

44. (Original) A delay-locked loop circuit as set forth in claim 36, wherein the phase comparison means adjusts amplitudes of the leading phase signal and the delayed phase signal according to a pulse amplitude adjusting signal.

45. (Original) A delay-locked loop circuit as set forth in claim 36, wherein

the phase comparison means selects at least one leading phase signal or delayed phase signal from a plurality of the leading phase signals or the delayed phase signals according to a pulse amplitude adjusting signal and outputs it to the first superposing means and the second superposing means,

the first superposing means includes at least one capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the first bias signal of the bias signal generating means at another terminal, and

the second superposing means includes at least one capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the second bias signal of the bias signal generating means at another terminal.

46. (Original) A delay-locked loop circuit as set forth in claim 36, wherein the phase comparison means adjusts pulse widths of the leading phase signal and the delayed phase signal according to a pulse width adjusting signal.